REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Continued Examination Under 37 C.F.R. § 1.114

Response to Amendment

In section 5 of the Office Action, the examiner objected to the amendment filed on August 20, 2002 under 37 C.F.R. § 132 because it introduces new matter into the disclosure. The Examiner stated:

> 37 C.F.R. § 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: claims 1, 11, 31 and 36 have been amended to include the feature "the distance causing the selected interference" or "the distance being predetermined to selectively cause interference." The applicant is respectfully reminded that the distance does not cause the interference. The interference between two light beams is caused by the phase difference between the two light beams.
>
> Applicant is required to cancel the new matter in the reply to this Office Action.

Applicants have amended claims 1, 11, 31, and 36 to remove the language that the Examiner asserted as new matter and to provide further clarity.

Drawings

In section 6 of the Office Action, the Examiner objected to the drawings under 37 C.F.R. § 1.83(a). The Examiner stated:

> The drawings must show every feature of the invention specified in the claims. Therefore, the features recited in claims 1, 11, 31 and 36 concerning the *substrate*, the *patterned optical lay with a plurality of optical pathway or conduits* and the *interference region* must be shown or the

> feature(s) cancelled from the claim(s). No new matter should be entered.
>
> A proposed drawings correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Applicant respectfully traverses the drawing objection, as FIG. 8 depicts a substrate 705 with a patterned optical layer 710. The interference regions patterned in layer 710 are depicted in FIGs. 1-5 as interference region 25 (FIGs. 1 and 2), interference region 325 (FIG. 3), interference regions 425 and 426 (FIG. 4) and interference region 525 (FIG. 5). Accordingly, Applicant requests that the drawings objection be withdrawn.

Not shown where is the [illegible] in Figs 1-5.

Claim Rejections 37 C.F.R. § 112

In section 8 of the Office Action, the Examiner rejected claims 1, 4-10, 11, 13-15, 17-22, 31, 33-36, and 38-46 under 37 C.F.R. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner stated, "[t]he reasons for rejection based on the newly added matters are set forth in the paragraph above."

Applicant has amended claims 1, 11, 31, and 36 as described above, for clarity.

In section 10 of the Office Action, the Examiner rejected claims 1 and 4-10 under 37 C.F.R. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner stated:

> The phrase "is representative of a Boolean logic output" recited in claim 1 is indefinite since it is not clearly what is considered here as the "representation". Claims 4-10 inherit the rejection from their based claim.

Independent claim 1 has been amended for clarity and thereby overcom s the indefiniteness rejection.

Claim Rejections - 35 U.S.C. § 103

In section 12 of the Office Action, The Examiner rejected claims 1, 4-10, 11, 13-15, 17-22, 36, and 38-46 under 35 U.S.C. § 103(a) as being unpatentable over the patent issued to Utaka et al. (U.S. Patent No. 5,315,422) in view of the patent issued to Yang (U.S. Patent No. 5,239,173). The Examiner stated:

> Utaka et al. teaches an *interference type optical logic element* for controlling optical signal by light, i.e., an *optical processor*, that is comprised of
>
> (1) a *substrate* (3) of a *first semiconductor material*, and
>
> (2) a *patterned optical layer* (7) overlaying the substrate of a *second semiconductor material.*
>
> Utaka et al. teaches that the optical layer (7) is patterned with a plurality of *optical waveguides* serve as the *optical pathways or optical conduits* (I and II) with at least one of the optical pathways receives an optical input light signal (P_I) and at least one of the optical pathways configured to provide an optical output light signal P_o), (please see Figures 2A, 2B, 3-5, 6A and 7-10). The input light signal propagates through the plurality of the waveguides or pathways to reach a region such that the light signals from the various waveguides interfere to each other wherein the interference causes the output light signal to perform a Boolean logical function, (please see columns 4-5). Utaka et al. teaches that the wavefronts of the light from the optical input signals via the optical conduits (I and II) intercept and interfere with each other at the region that two conduits meets, which is identified as interference region, (please see Figure 2A).
>
> The input optical signals via either the optical conduits I or II, of Utaka et al., may be identified as the bias optical signal. Since as defined by the applicant the bias optical signal referred here is a *light signal* and Utaka et al. also teaches that the input optical signals are provided as light signal (P_o, column 3). Also the bias optical signal as one of the input

optical signals must interfere with the other input signal to make the logic gate operable, this means the bias optical signal has to be **coherent** to the other input optical signal. The two input optical signals pass through the two conduits (I and II) of Utaka et al. are generated as light input signals and are coherent to each other, it is therefore implicitly true that one of the signals can be identified as the bias optical signal.

Claims 1, 11 and 36 have been amended to make the two optical paths or optical conduits being separated by a distance at the entrance of the interference region. Yang in the same field of endeavor teaches an optical logic device that is comprised of at least two optical pathways or conduits for inputting input light signals into an interference region to allow the two light signals going through desired interference to perform the desired optical logic operation. Yang teaches that the optical pathways can be designed to have a distance separation between them at the entrances of the interference region, (please see Figures 5-6). It would have been obvious to one skilled in the art to apply the teachings of Yang to modify the optical logic element of Utaka et al. for the benefit of producing a different design for performing the same logic operations.

With regard to claims 4-8 and 38-42 Utaka et al. teaches that the patterned optical layer may have two or three waveguides or pathways for receiving optical input light signal to perform various logical operations including AND, NAND, OR XOR, NXOR. This reference (Utaka et al.) does not teach explicitly to have the NOT logic function. Yang teaches that the optical logic device is capable to perform NOT logic function. It would then have been obvious to one skilled in the art to modify the optical logic element of Utaka et al. according to Yang for the benefit of adding NOT logic function to the logic operation of the optical logic element.

With regard to claims 9-10 and 44-45, Utaka et al. teaches that the optical logic element is used as *optical processor* for processing and controlling optical signals, Utaka et al. also teaches that a plurality of optical logic elements may be integrated such that a combination of basic logic functions (AND, OR and NOT) can be achieved to provide more complicated logic function such as NAND, XOR and NXOR. Although this reference does not teach explicitly to have the combined NOT and NAND functions such modification would

have been obvious to one skilled in the art since it simply involves combining these elements for the purpose of performing the desired logic function.

With regard to claims 13-16, Utaka et al. teaches that the patterned optical layer may have two or three waveguids or conduits for receiving optical input light signal to perform various logical operations such as AND, NAND, OR, XOR, NXOR. However this reference does not teach explicitly that the input signals are biased. This feature is rejected for the reasons stated above. It also does not teach explicitly that the logic function is NOT. Yang teaches that the optical logic device is capable to perform NOT logic function. It would then have been obvious to one skilled in the art to modify the optical logic element of Utaka et al. according to Yang for the benefit of adding NOT logic function to the logic operation of the optical logic element.

With regarding to claims 17-20, Utaka et al. teaches that the optical layer or the substrate may be formed by doped Gallium Arsenide, (please see column 1). However it does not teach explicitly that it may also be formed by doped silicon. However doped silicon is a very well known semiconductor material for making logic circuit in the art and since the specification fails to teach the criticality of having this particular material would overcome any problem in the prior art such modification would have been obvious matter design choice to one skilled in the art.

With regard to claims 21 and 22, Utaka et al. teaches that a semiconductor DFB laser may be used as the light source to provide the input light signals, (please see Figure 8A and column 8).

With regard to claims 43 and 46, Utaka et al. teaches that the optical logic element may perform logic functions such as NAND and XOR, (please see column 8).

Always

With regard to independent claim 1, neither Utaka et al. nor Yang alone, or in any proper combination, disclose, teach or suggest, "a first optical pathway configured to transmit an optical bias signal having a wavelength and a phase" and "a second optical pathway configured to provide a modulated optical input signal having the same wavelength and phase as the optical bias signal." Utaka et al. discloses an input signal P_i

Not disclose

Not disclosed.

which is divided along the path I and II, the signal traveling along path I is changed in phase by a modulating element (MOW 4, see FIG. 2) which is controlled by an optical control signal P_1. Similarly, optical signal P_i traveling along the pathway II has its phased changed by a modulating element (MOW 4', see FIG. 2) which is controlled by an optical control signal P_2. Accordingly, the inputs to the "interference region" described by the Examiner are P_{i_1} and P_{i_2} which do not have the same phase in contrast to the optical logic circuit recited in amended independent claim 1. Not supported

Interference always based on locations

Further, the interference produced in Utaka et al. is not based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways. Further, the location of the third optical pathway is <u>not a function of the wavelength and the length of the</u> interference region and the distance between the first and second optical pathways. Whereas the interference region of Utaka et al. depends on the phase difference between P_{i_1} and P_{i_2}, the interference region of independent claim 1 is dependent upon the location of the first optical pathway with respect to the second optical pathway and the location of the third optical pathway relative to the first and second optical pathways and the phase of the input signals being the same. Further still, Utaka et al. teaches phase modulation to achieve the desired interference. As claim 1 recites the optical signals are of the same phase, thus there is no phase modulation. Accordingly, the combination of Yang and Utaka et al. do not teach, disclose, or suggest alone, or in any proper combination, all of the elements of independent claim 1. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. <u>In re Royka</u>, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Not taught

Further still, even if all of the elements of independent claim 1 could be found in Utaka et al. and Yang, there is no motivation or suggestion to combine the teachings of Utaka et al. and Yang to produce the combination recited in independent claim 1. Utaka et al. does not provide for any desirability to combine the interference region of Yang with

the optical logic element disclosed in Utaka et al. to form the combination recited in independent claim 1. Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

According, independent claim 1 and its dependents are not obvious in view of Utaka et al. and Yang.

With regard to independent claim 11, neither Utaka et al. nor Yang alone, or in any proper combination, disclose, teach or suggest, "a patterned optical layer overlying the substrate at least partially configured of a second material, the patterned optical layer providing a plurality of optical conduits of the second material, at least two of the optical conduits configured to receive optical input signals, each of the optical input signals having the same phase, at least one of the optical conduits configured to provide optical output signals, and at least one of the at least two optical input signals being an optical bias input signal." Utaka et al. discloses an input signal P_i which is divided along the path I and II, the signal traveling along path I is changed in phase by a modulating element (MOW 4, see FIG. 2) which is controlled by an optical control signal P_1. Similarly, optical signal P_i traveling along the pathway II has its phased changed by a modulating element (MOW 4', see FIG. 2) which is controlled by an optical control signal P_2. Accordingly, the inputs to the "interference region" described by the Examiner are P_{i_1} and P_{i_2} which do not have the same phase in contrast to the optical logic circuit recited in amended independent claim 11.

Further, the interference produced in Utaka et al. is not based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways. Further, the location of the third optical pathway is not a function of the wavelength and the length of the interference region and the distance between the first and second optical pathways. Whereas the interference region of Utaka et al. depends on the phase difference between P_{i_1} and P_{i_2}, the interference region of independent claim 11 is dependent upon the location of the first optical pathway with respect to the second optical pathway and the location of the third optical pathway relative to the first and second optical pathways and the phase of the input signals being the same. Further still, Utaka et al. teaches phase modulation to achieve the desired interference. As claim 11 recites the optical signals are of the same phase, thus there is no phase modulation. Accordingly, the combination of Yang and Utaka et al. do not teach, disclose, or suggest alone, or in any proper combination, all of the elements of independent claim 11. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Further, even if all of the elements of independent claim 11 could be found in Utaka et al. and Yang, there is no motivation or suggestion to combine the teachings of Utaka et al. and Yang to produce the combination recited in independent claim 11. Utaka et al. does not provide for any desirability to combine the interference region of Yang with the optical logic element disclosed in Utaka et al. to form the combination recited in independent claim 11. Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific

combination that was made by the applicant. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

According, independent claim 11 and its dependents are not obvious in view of Utaka et al. and Yang.

With regard to independent claim 36, neither Utaka et al. nor Yang alone, or in any proper combination, disclose, teach or suggest, "an optical layer overlaying the substrate at least partially comprising a second material, the optical layer being patterned to provide a plurality of optical pathways, at least two optical pathways configured to provide optical input signals, the optical input signals being of the same phase, and at least one optical pathway configured to provide an optical output signal." Utaka et al. discloses an input signal P_i which is divided along the path I and II, the signal traveling along path I is changed in phase by a modulating element (MOW 4, see FIG. 2) which is controlled by an optical control signal P_1. Similarly, optical signal P_i traveling along the pathway II has its phased changed by a modulating element (MOW 4', see FIG. 2) which is controlled by an optical control signal P_2. Accordingly, the inputs to the "interference region" described by the Examiner are P_{i_1} and P_{i_2} which do not have the same phase in contrast to the optical logic circuit recited in amended independent claim 36.

Further, the interference produced in Utaka et al. is not based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways. Further, the location of the third optical pathway is not a function of the wavelength and the length of the interference region and the distance between the first and second optical pathways. Whereas the interference region of Utaka et al. depends on the phase difference between P_{i_1} and P_{i_2}, the interference region of independent claim 36 is dependent upon the location of the first optical pathway with respect to the second optical pathway and the location of

the third optical pathway relative to the first and second optical pathways and the phase of the input signals being the same. Further still, Utaka et al. teaches phase modulation to achieve the desired interference. As claim 36 recites the optical signals are of the same phase, thus there is no phase modulation. Accordingly, the combination of Yang and Utaka et al. do not teach, disclose, or suggest alone, or in any proper combination, all of the elements of independent claim 36. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Further, even if all of the elements of independent claim 36 could be found in Utaka et al. and Yang, there is no motivation or suggestion to combine the teachings of Utaka et al. and Yang to produce the combination recited in independent claim 36. Utaka et al. does not provide for any desirability to combine the interference region of Yang with the optical logic element disclosed in Utaka et al. to form the combination recited in independent claim 36. Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

According, independent claim 36 and its dependents are not obvious in view of Utaka et al. and Yang.

In section 13 of the Office Action, the Examiner rejected claims 31, and 33-35 under 35 U.S.C. § 103(a) as being unpatentable over the patent issued to Yang in view of Utaka et al. The Examiner stated:

Yang teaches a binary data processor for providing various logical functions wherein the processor comprises a coherent light source (11) for providing light through light pipes (41) serve as the plurality of optical pathways and slits (13 and 14) serves as the optical inputs to a portion such that the light from the plurality of pathways or light pipes interfere with each other, (please see Figures 4 and 5, column 4). The interference pattern is transmitted via output light pipes (42) or fiber optic bundle (43) as the optical output light signal may represent various logic functions such as AND, OR and NOT. Claim 31 has been amended to include the feature that a distance separation is set between the pluralities of pipes at the entrance of the interference regions. Figure 4 shows explicitly that at the entrances of the interference region the inputs and the light pipes are separated by a distance. The distance is implicitly predetermined to make the processor capable of performing the intended optical logic functions.

This reference has met all the limitations of the claims with the exception that it does not teach explicitly that the data processor is formed of optical transmission material patterned on a substrate material. It is extremely well known in the art to form optical logic circuit on a waveguide arrangement with patterned optical waveguides or pathways in a transmission optical material on a substrate material such is demonstrated by the teachings of Utaka et al. with patterned optical layer (7) on a substrate (3), (please see Figure 2A). It would then have been obvious to one skilled in the art to apply the teachings of Utaka et al. to make the data processor with optical logic functions on a waveguide arrangement for the benefit of making it suited for desired applications.

Yang further teaches that logic circuit system having multiple logic steps can be constructed from combination of basic logic functions AND, OR and NOT. In Figure 6, Yang teaches a data processor system having a *cascaded series* of N optical processing steps that may include various combinations of the basic logic functions. Although this reference does not teach explicitly to have NOT AND (NAND) function and to have NOT and NOT AND function however since these functions are combinations of the basic logic functions, they are therefore either implicitly included or obvious modifications to one skilled in the art for the benefit of providing additional logic functions.

With regard to independent claim 31, neither Yang nor Utaka et al. discloses, teaches, suggests, or provides any motivation for the combination to provide all of the limitations recited in independent claim 31. Independent claim 31 recites "providing an optical bias input signal to a first optical input such that the optical bias input signal is in an always on condition." Neither Yang nor Utaka et al. discloses, teaches, suggests, or provides any motivation for providing an optical bias signal in combination with a second selective optical input signal. Yang teaches the use of a plurality of electro-optical shutters 15 (see FIG. 1) which provide for the selective input of optical signals into the multi-partitioned chamber 17. Because independent claim 31 recites that the plurality of optical pathways are formed of optical transmission material patterned on a substrate material, Yang provides no motivation for such forming of optical pathways because electro-optical shutters could not be incorporated into patterned optical pathways of optical transmission material patterned on a substrate material as recited in independent claim 31. For the operation of Yang, the electro-optical shutters are necessary. Accordingly, there is no teaching or suggestion to combine the teachings of Yang and Utaka et al. to provide the optical bias input signal and the second selective optical input signal which are provided in optical pathways formed of optical transmission material and provided as inputs to an interference region, where the interference region enables selective interference of the optical bias input signal and the second selective optical input signal.

Accordingly, there is no teaching of a combination of elements by Yang and Utaka et al., either alone, or in any proper combination. Therefore, independent claim 31 and its dependent claims are allowable.

* * *

After amending the claims as set forth above, claims 1-22 and 31-46 are now pending in this application.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date January 20, 2003

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MARKED UP VERSION SHOWING CHANGES MADE

Below are the marked up amended claim(s):

1. (Thrice Amended) An optical logic circuit, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate at least partially comprising a second material, the optical layer configured to provide a plurality of optical pathways, [at least one] the optical pathways including a first optical pathway configured to transmit an optical bias signal having a wavelength and a phase, [at least one] a second optical pathway configured to provide [an] a modulated optical input signal having the same wavelength and phase as the optical bias signal, and [at least one] a third optical pathway configured to provide an optical output signal; and

an interference region at least partially comprising the second material, configured to selectively cause interference of wavefronts of the optical bias signal and the modulated optical input signal entering the interference region, [the interference being caused by the distance between the optical pathway configured to transmit the optical bias signal and the optical pathway configured to provide the optical input signal, at the entrance to the interference region,] the interference being based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways, the location of the third optical pathway being a function of the wavelength and the length of the interference region and the distance between the first and second optical pathways,

wherein the optical output signal is [representative of] a Boolean logic output signal based on the [at least one] optical input signal and the optical output signal exits an interference region output.

4. (Twice Amended) The optical logic circuit of claim 1, wherein the interference region is configured to cause substantial cancellation of light exiting the

interference region when light is provided to the interference region in the form of the modulated optical input signal.

5. (Twice Amended) The optical logic circuit of claim 1, wherein the interference region includes a first selective optical input receiving the modulated optical input signal and a second selective optical input receiving a second modulated optical input signal.

11. (Thrice Amended) An optical logic gate for an optical processor, comprising:

a substrate configured of a first material;

a patterned optical layer overlying the substrate at least partially configured of a second material, the patterned optical layer providing a plurality of optical conduits of the second material, at least two of the optical conduits configured to receive optical input signals, each of the optical input signals having the same phase, at least one of the optical conduits configured to provide optical output signals, and at least one of the at least two optical input signals being an optical bias input signal; and

an interference region coupled to at least two of the optical conduits configured to receive optical input signals, [the at least two of the optical conduits entering the interference region and being separated by a distance, the distance causing] selective interference being caused along a predetermined axis in the interference region, the interference being based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways, the location of the third optical pathway being a function of the wavelength and the length of the interference region and the distance between the first and second optical pathways, and the interference region being coupled to at least one of the optical conduits configured to provide optical output signals,

wherein the interference region is configured to provide a Boolean logic output signal based on the at least one optical input signal.

31. (Thrice Amended) A method of providing a B olean logic optical output signal based on at least two optical input signals, comprising:

providing [a first selective optical] an optical bias input signal to a first optical input such that the optical bias input signal is in an always on condition;

providing a plurality of optical pathways formed of optical transmission material patterned on a substrate material;

providing a second selective optical input signal; [and]

providing a distance between the plurality of optical pathways entering the interference region, the [distance being predetermined to selectively cause interference between wavefronts of the first selective optical bias input signal and the second optical input signal] interference region enabling selective interference of the optical bias input signal and the second selective optical input signal along a predetermined axis in the interference region, the interference being based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways, the location of the third optical pathway being a function of the wavelength and the length of the interference region and the distance between the first and second optical pathways; and

providing an optical output signal, the optical output signal based on the at least two input signals and representative of a Boolean logic function.

36. (Thrice Amended) An optical logic circuit, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate at least partially comprising a second material, the optical layer being patterned to provide a plurality of optical pathways, at least two optical pathways configured to provide optical input signals, the optical input signals being of the same phase, and at least one optical pathway configured to provide an optical output signal; and

an interference region configured to selectively cause interference of wavefronts of light from the optical input signals entering the interference region [by

having the at least two optical pathways providing an input, being separated by a distance, the distance being predetermined to cause], the interference being based on the location of the first optical pathway with respect to the second optical pathway entering the interference region and the length of the interference region and the location of the third optical pathway relative to the first and second optical pathways, the location of the third optical pathway being a function of the wavelength and the length of the interference region and the distance between the first and second optical pathways, the selective interference being produced along a predetermined axis in the interference region[;],

wherein the interference region is configured to provide a Boolean logic output signal based on the at least two optical input signals.